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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/070,535	03/07/2002	Franz Hutner	449122023600	5551

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EXAMINER	
LEE, CHRISTOPHER E	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 08/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/070,535	HUTNER ET AL.	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 March 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/7/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the Preliminary Amendment filed on 7th of March 2002. No claim has been amended; claims 1-9 have been canceled; and claima10-18 have been newly added. Currently, claims 10-18 are pending in this application.

Specification

2. The disclosure is objected to because of the following informalities:

On page 1, line 11, substitute "apparstus" by --apparatus--.

On page 8, line 30, substitute "module 2" by --module 4--.

Appropriate correction is required.

Drawings

3. The drawing is objected to because the module 2 in Fig. 2 has a configuration of request lines connection for the module 4. Thus, the module 2 in Fig. 2 should be corrected to module 4. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and

informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claims 11-15, 17 and 18 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. The claims' dependency numberings are incorrect. The Examiner assumes their correct dependencies in light of the specification for the purpose of the claim rejection based on prior art.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 10-12, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fisch et al. [US 5,901,297 A; cited by the Applicants; hereinafter Fisch] in view of what was well known in the art, as exemplified by Yoon [US 5,898,847 A].

Referring to claim 16, Fisch discloses a system (i.e., multiprocessor computer system in Fig. 1) for interchanging data between modules (i.e., Processor(0) - Processor (n) in Fig. 1) connected to a common bus (i.e., Processor-Memory Bus 101 of Fig. 1; See col. 4, lines 26-27), comprising: request lines (i.e., BREQ0# 311 - BREQ3# 314 in Fig. 3), which respectively connect one module to said other modules, to transmit bus request information (See col. 7, lines 46-47); a request memory (i.e., Agent ID 325 and Arbitration Counter 330 in Fig. 3) in each of said modules to store a clock cycle of an output (i.e., counter value in Arbitration Counter 330 of Fig. 3) and an origin of said bus request information (i.e., agent identifier in Agent ID 325 of Fig. 3); a bus use circuit (i.e., Comparator 340 of Fig. 3) in each of said modules to control bus use by a respective module on said basis of said bus request information stored in said request memory (See col. 7, lines 58-59; i.e., wherein in fact that each agent determines the owner of the bus based on the value of its own arbitration counter anticipates each of said modules to control bus use by a respective module on said basis of said bus request information stored in said request memory) in line with a decision pattern which is prescribed and identical for said modules (See col. 6, lines 60-67; e.g., counter value 0 or any particular non-zero value).

Fisch does not expressly teach a timer line, connected to said modules, to synchronize said modules.

The Examiner takes Official Notice that said system comprising a timer line (i.e., bus clock BCLK* in Fig. 3 of Yoon), connected to said modules (i.e., bus agents MPU 2, SMU 3, IOU 4 and SCU 5 in Fig. 1 of Yoon), to synchronize said modules, is well known to one of ordinary skill in the art, as evidenced by Yoon at col. 4, lines 26-32).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have included said timer line (i.e., bus clock line) in said system (i.e., multiprocessor system) so as to synchronize said modules (i.e., bus agents).

Referring to claim 17, Fisch teaches a line to transmit a reset signal (i.e., RESET# in Fig. 3) which puts said request memories into a standard initial state (See col. 7, lines 19-33).

Referring to claim 10, the method steps of claim 10 are inherently performed by the apparatus of claim 16, and therefore the rejection of claim 16 applies to claim 10.

Referring to claim 11, Fisch teaches resetting said request memories into an identical initial at the start of said method (See col. 7, lines 19-33 and col. 10, line 66 through col. 11, line 17).

Referring to claim 12, Fisch teaches said bus (i.e., Processor-Memory Bus 101 of Fig. 1) is operated by said plurality of modules (i.e., Processor(0) - Processor (n) in Fig. 1) in the order in time in which the corresponding bus request information was output on the basis of said decision pattern (See col. 7, lines 1-12).

8. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fisch [US 5,901,297 A] as applied to claims 10-12, 16 and 17 above, and further in view of Spencer et al. [US 4,161,779; cited by the Applicants; hereinafter Spencer].

Referring to claim 13, Fisch discloses all the limitations of the claim 13 except that does not teach if said plurality of modules output bus request information at the same time in a clock cycle, the corresponding information is stored in a shared memory block in said request memory, and said bus is used in a prescribed order on the basis of information stored in a memory block. Spencer discloses a dynamic priority system (See col. 1, lines 7-10), wherein if a plurality of modules (i.e., a plurality of stations 15, 23 and 31 in Fig. 1) output bus request information at the same time in a clock cycle (See Abstract), the corresponding information (i.e., count up by one value for a waiting device) is stored in a shared memory block (i.e., Queue Counter 53 of Fig. 2) in a request memory (i.e., Queue Counter 53 and Race Counter 57 in Fig. 2), and a bus (i.e., Data 49 of Fig. 2) is used in a prescribed order on the basis of information stored in a memory block (See col. 3, lines 15-56).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said interfacing logic for processing said concurrent device requests with said necessary components, as disclosed by Spencer, in said module (i.e., bus agent), as disclosed by Fisch, for the advantage of providing a dynamic priority ordering system for granting a plurality of requesting modules (i.e., stations) access to said module (i.e. shared device) in the order of their request (See Spencer, col. 1, lines 56-59).

Referring to claim 14, Spencer teaches said plurality of modules output no additional bus request information if the number of said at least partly used memory blocks has reached a prescribed limit value (See col. 3, lines 44-47; i.e., wherein in fact that the memory is instructed to transfer the data (i.e., bus granted) stored therein over line (i.e., data bus) if it is terminal that has reaches the maximum count first implies that said plurality of modules (i.e., bus waiting modules except the bus granted module) output no additional bus request information if the number of said at least partly used memory blocks (i.e., Race Count value) has reached a prescribed limit value (i.e., when the Race Counter reaches the maximum count, its terminal is granted to use the data bus, and thus other terminals output no additional bus request)).

9. Claims 15 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fisch [US 5,901,297 A] as applied to claims 10-12, 16 and 17 above, and further in view of Cubranich et al. [US 5,051,946; cited by the Applicants; hereinafter Cubranich].

Referring to claim 18, Fisch discloses all the limitations of the claim 18 except that does not teach each module has another memory for higher priority bus request information which is output by at least one of said modules, said bus use circuits taking into account said higher priority bus request information stored in said another memory on the basis of a prescribed use algorithm.

Cubranich discloses an integrated scannable rotational priority network apparatus (See Abstract and Fig. 2), wherein a module (e.g., central processor 14 of Fig. 1) has a memory (i.e., priority

Encode/Blocking Network 74 of Fig. 2) for higher priority bus request information (i.e., pre-emptive priority request) which is output by at least one of modules (i.e., output via request line 20 in Fig. 2), bus use circuits (i.e., Section D in unit 18 of Fig. 2) taking into account said higher priority bus request information stored in said memory on the basis of a prescribed use algorithm (See col. 5, lines 7-20).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said algorithm (i.e., logic for processing higher priority bus request information) with said necessary components, as disclosed by Cubranich, in said module (i.e., bus agent), as disclosed by Fisch, so as to block a request grant signal for said individual module (i.e., unit) after having logically determined that a higher priority bus request information (i.e., higher order priority request) is active (See Cubranich, col. 5, lines 17-20).

Referring to claim 15, the method steps of claim 15 are inherently performed by the apparatus of claim 18, and therefore the rejection of claim 18 applies to claim 15.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

IBM TDB [Account No. NN9204200] discloses Multi-Processor Bus distributed arbitration with centralized fairness.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 703-305-5950. The examiner can normally be reached on 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christopher E. Lee
Examiner
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cel/

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